

SYSTEM AND METHOD FOR CLAMP CURRENT REGULATION OF INDUCTION MACHINES

Background of the Invention

Technical Field

5 The present invention is directed generally to electromechanical machines, and, in particular, to a system and a method for current regulation in the field-weakening operation of induction machines.

Description of the Related Art

10 In the control of inverter-driven induction machines, field weakening is often used to lower the inverter voltage rating for a given application. Without field weakening the inverter manufacturer would have to use components rated to handle higher levels of voltage for that given application. This would undesirably add incremental costs to the drive system. During high speed operation, the phase current may be applied to the machine windings in advance of the phase electromotive force.

15 To control the electromotive force, the D axis current is decreased inversely with speed.

 It is known to provide a flux weakening algorithm by the use of a number of look-up tables to produce the reference Q-axis and D-axis currents. However, the use of look-up tables requires the creation of numerous and

20 cumbersome data structures within the look-up tables themselves to handle all possible situations in the system and its environment.

 Accordingly, there is a need for a current control system that minimizes or eliminates one or more of the above-mentioned shortcomings.

Summary of the Invention

25 The invention is based upon the discovery that in current control for induction machines, a limiter in the current regulator of a proportional integral control that clamps the current regulators at the available voltage vector with appropriate phase preventing loss of current regulation, maximizes the efficiency of the machine and produces maximum torque in the field weakening region. The arrangement is

30 capable of adjusting to the true base speed of the machine as the DC-link voltage varies.

The invention is directed to a device for regulating current produced in an induction machine responsive to a plurality of phase current signals for producing torque at the machine output shaft. The device includes a processing and drive circuit responsive to a direct current command signal and a quadrature current command
5 signal for producing a plurality of phase current signals at the input to the machine. A command circuit is responsive to the phase current signals and an angular position of the shaft for producing a direct current error signal and a quadrature current error signal. A control circuit is responsive to the direct and quadrature current error signals to produce the direct and quadrature voltage modulation index signals. The
10 control circuit includes a proportional controller and integrator responsive to each of the direct and quadrature current error signals. The proportional controller and integrator outputs are summed and fed back to the command circuit. A limiter is located in the feed back loop to clamp the summed outputs at the available voltage vector and provide appropriate phase.

15 The method according to the invention limits current regulators to an available voltage magnitude, voltage angle delta and a slip frequency range for assuring that the system does not exceed the available voltage and that the machine efficiency is maximized and that maximum torque is produced in the field-weakening region.

20 Other features, objects and advantages of the present invention will become apparent to one of ordinary skill in the art from the description that follows and may be realized by means of the instrumentalities and combinations particularly pointed out in the appended claims, taken in conjunction with the accompanying drawings.

25 Brief Description of the Drawings

The present invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Fig. 1 is a schematic block diagram of an induction machine drive employing exemplary control system according to the invention.

30 Fig. 2 illustrates an exemplary current clamp command employed in the circuit of Fig. 1.

Fig. 3 is a flow chart showing the implementation of a limiting algorithm employed in the circuit of Fig. 2.

Description of the Invention

The invention is directed to a method and apparatus for current control in induction machines. The method is specifically designed to produce additional functionality in the field-weakening region.

To extend the operational speed range of induction machines, it is necessary to de-flux the machine by applying reduced current in the synchronous D-axis, I_{ds} . The advantage of the method is that it applies the appropriate amount of current at each operating point across the entire speed range of the machine, that is, in the constant torque region and in the field-weakening region.

An important feature of the invention is that when the current regulator exceeds the available voltage, the system decreases I_{ds} . Furthermore, when the voltage angle exceeds the maximum voltage angle δ for motoring mode, or is less than the minimum voltage angle δ for generating mode, the system clamps the angle to the maximum δ angle for motoring mode or the minimum δ angle for generating mode, and the slip frequency is kept to the value that provides maximum torque for motoring or minimum torque for generating mode. As a result, the current regulator does not run out of voltage, maximizes the machine efficiency and provides maximum torque in the field-weakening region for motoring mode, or minimum torque in the field weakening region for generating mode,

It is important to note that the base-speed of a machine changes significantly depending upon variations in the DC-link voltage. However, the invention is able to properly identify the base-speed so that the constant torque region is extended to as high a speed as possible.

Fig. 1 shows a block diagram of an exemplary system 10 according to the invention. The apparatus is adapted for controlling an induction machine 12, e.g. a motor/generator, having a stator S and a rotor R for driving a shaft. The machine is driven by a three phase inverter 14 coupled to a DC-link voltage source 16 (Vdc). Vdc is sometimes herein after referred to as the link voltage. A pulse width modulator (PWM) 18 drives the inverter in a known way.

Control of the induction motor may be implemented by a digital signal processor (DSP). Such DSPs are known and are arranged to be responsive to various inputs for producing control outputs, for driving the motor according to the invention. A sensor S0 is coupled to the motor 12 to produce a sensor rotor position signal θ_r .

5 The sensed rotor position signal θ_r is coupled to a theta synchronous block 20 which produces synchronous angle signal θ_e . The output of block 20 is coupled to coordinate transform circuits 22 and 24, as shown. The coordinate transform 22 transforms D-axis and Q-axis modulation index signals to produce modulation index signals in stationary coordinates α and β . The modulation index signals in the
10 stationary coordinate frame are coupled to and modulated by a space vector modulator 26 in a known manner to produce outputs that drive the voltage PWM modulator 18. PWM modulation block 18 generates the gate drive signal for inverter 14, which provides voltage to machine 12.

Motor drive phase currents a, b and c to the machine 12 from inverter
15 14 drive the motor 12. These are coupled in feed back relation to the coordinate transform 24 which transforms motor drive stationary current from the inverter 14 to direct and quadrature synchronous axis signals I_{dsf} and I_{qsf} . These signals are likewise coupled to the theta synchronous block 20 as shown, and to adders 34 and 36 in the current clamp regulator circuit 30.

20 The current clamp regulator 30 includes an I_{ds} current command block 32 and an I_{qs} current command block 33 which calculate direct and quadrature current commands I_{ds}^* and I_{qs}^* respectively (Commands are designated by an asterisk (*)). The current commands I_{ds}^* and I_{qs}^* are summed with the respective transformation feedback output I_{dsf} and I_{qsf} at summing nodes 34 and 36
25 respectively. I_{ds}^* and I_{qs}^* are each coupled to the non inverting inputs of respective summing nodes 34 and 36. Likewise I_{dsf} and I_{qsf} are coupled to the inverting inputs of respective nodes 34 and 36. The summed signals respectively represent the D-axis current error signal I_d error and the Q-axis current error signal I_q error. The error signals are coupled to corresponding proportional-integral (PI) current regulators 38
30 and 40. The outputs of the PI regulators represent the D-axis voltage V_{ds} and the Q-axis voltage V_{qs} respectively. These signals are coupled to the transform circuit 22 for appropriate transformations as noted above. The voltage signals V_{ds} and V_{qs} are

also fed back to the I_{ds} current command block 32 as shown and are coupled to the theta synchronous block 20.

The PI current regulators 38 and 40 include limiters for clamping the D-axis and Q-axis modulation index signals V_{ds} and V_{qs} to some limited voltage with a given limited angle delta in order to prevent an undesirable loss of current regulation, to maximize machine efficiency and to provide maximum torque in the field weakening region.

The current command circuit 32 receives a Torque* command input, and a zero vector time control command signal $T0^*$ as an input. Alternatively, the current command circuit 32 may receive the addition of time 1 and time 2 vectors as a control signal, i.e., $(T1+T2)^*$ or the voltage magnitude command signal V_{MAG}^* . The I_{ds} current command circuit 32 receives a feedback signal corresponding to the zero vector time $T0$ from space voltage modulator 26. Feedback signal from the space modulator 26 may be in the form of the sum of vectors 1 and 2 i.e. $(T1+T2)$ or

according to a known relationship, namely $V_{MAG} = \sqrt{V_{ds}^2 + V_{qs}^2}$.

Fig. 2 illustrates a block diagram of the clamp arrangement employed in the proportional integrators 38 and 40. As illustrated, for the D-axis, the zero time vector $T0$ is fed back from the space vector modulator 26 and is input to a ripple filter 42. The output of filter 42 is time zero feedback output $T0f$ which is summed at the non-inverting input of node 44. The zero time vector control $T0^*$ is coupled to the inverting input of the node 44. The difference is error signal $T0e$ which is coupled to a proportional integrator (PI) circuit 46 and which feeds limiter or clamp 48. The clamp 48 has a feedback loop of 50 which is coupled to the PI circuit 46 as shown. The limiter 48 produces an output $I_{ds}T0$ which is limited to values less than or equal to zero.

The output $I_{ds}T0$ of the limiter 48 is summed at node 54 with a look up table ($I_{ds}LUT$) output for I_{ds} from maximum torque per amp curve block 52 both of which are non-inverted, as shown, to produce the D axis current control signal I_{ds}^* . Block 52 is fed by the Torque* control signal.

The I_{ds}^* signal and I_{dsf} feedback signal are summed at the respective non-inverting and inverting inputs of node 34 to produce I_d error, which is coupled to parallel connected proportional circuit 56 and integrating circuit 58. Proportional

circuit 56 produces one output which is coupled to the non-inverting input of summing node 60. The integrating circuit 58 also coupled to the node 34 is, in turn, coupled to a clamp or limiting circuit 62 having a feedback loop 64 as shown.

The proportional circuit 56 controls the transient components of the Id error signal, and the integrating circuit 58 controls steady state components of the Id error signal. The clamp 62, when implemented, is used to limit the steady state value within an allowable range. The output of the clamp 62 is coupled to another non-inverting input of the summing node 60. The output of the node 60 is the unclamped D-axis modulation index signal Vds. This signal is coupled to clamp or limiting circuit 66, and when engaged, the output of the clamp 66 is the clamped D-axis modulation index signal Vds. As shown in Fig. 1, the Vds signal is coupled to the transform circuit 22 and is fed back to the current command circuit 32 and the theta synchronous block 20. The second clamp 66 limits the overall output Vds.

Iqs current command block 33, Fig 2., produces Iqs* command signal in response to the torque command signal Torque* and feedback signal Idsf from transform block 24. The Q-axis reference or command signal Iqs*, Fig. 2, is coupled to the non-inverting input of the node 36. The Iqsf feedback signal from the transform circuit 24 is coupled to the inverting input of the node 36. The node 36 produces an Iq error signal. The Iq error signal is coupled to proportional controller 70 and the integrator 72. Proportional circuit 70 produces transient signals and the integrating circuit 72 produces steady state signal. The output of the proportional control 70 is coupled to the non-inverting input of a node 74. The output of the integrator 72 is coupled to a clamp 76. The clamp 76, when implemented, is used to limit the steady state value within an allowable range. The output of the clamp 76 is coupled to another non-inverting input of summing node 74 and is fed back over line 78 to integrator 72, as shown. The signals are summed at node 74, and the output of the node 74 is the unclamped Vqs. This signal is coupled to clamp or limiting circuit 80, and when engaged, the output of the clamp is clamped Q-axis modulation index signal Vqs. This, in turn, is coupled to the transform circuit 22 and is fed back to the current command circuit 32 and the theta synchronous block 20 as shown in Fig. 1. The second clamp 80 limits the overall output Vqs.

When activated, clamps 66 and 80 limit the overall D and Q axis signals. Clamps 62 and 76 limit or clamp the steady state signals. The limiting or

clamping circuits illustrated in Fig. 2 thereby result in the protections and versatility afforded by the circuit of the present invention.

Activation of clamps 66 and 80 occurs when the unclamped Vds, in combination with unclamped Vqs is out of a selected voltage vector range. i.e. magnitude and direction (delta angle). Once engaged, clamps 66 and 80
5 corresponding clamps 62 and 76 are operative through feedback lines 67 and 81 to implement an algorithm exemplified in Fig. 3 to limit Vds and Vqs to the clamped values as shown.

Fig. 3 is a flow chart which illustrates a flow chart for implementing an
10 algorithm for initiating clamping action of the apparatus of the present invention. The unclamped direct and quadrature voltage signals Vds and Vqs are used to calculate the delta angle in block 80. The delta angle is $(\arctan(-V_{ds}/V_{qs}))$. The delta angle signal of block 80 is compared with a delta max lookup signal of block 82 in comparator block 84. The delta max look-up signal is derived by examining the rotor
15 speed W_r produced by differential circuit 86 in response to the rotor position signal θ_r , as shown.

If the delta angle is greater than or equal to the delta max, as sensed at block 84, then Vds and Vqs are recalculated via blocks 110, 88, 90 and 92, as shown. The output of block 92 represents the clamped D and Q axis signals. The function of
20 blocks 110 and 88 are discussed below. If the delta angle is less than the delta max, as determined at block 84, then a No Change output is produced at block 94. The No Change output is coupled to the block 92 which produces Vds and Vqs outputs which are unclamped.

As further illustrated in Fig. 3, if the delta angle is greater than the
25 delta max, as determined in block 84, then the Slip Frequency Max. look up block 96 provides the slip frequency W_{slmax} in response to the rotor speed signal W_r derived from differentiating block 86. The maximum slip frequency of block 96 sets the value in block 98 and inputs this to block 104 for summation with the rotor frequency W_r . If the delta angle is not greater than delta max (Block 84), then the slip frequency
30 W_{sl} is calculated from feedback currents I_{dsf} and I_{qsf} via blocks 100 and 102. The slip frequency is added to rotor frequency to obtain synchronous frequency W_e in block 104. The output of 104 is integrated at 106 to produce a synchronous position

output signal θ_e . The synchronous position signal θ_e is employed as an input to transform circuits 22 and 24 (Fig. 1).

In addition, block 110 may be responsive to the affimator output of Delta max block 84. Block 110 determines if the Iq error signal is greater than or equal to a minimum value of the Iq error. An affirmative comparison is coupled to
5 block 88 where Delta Angle is set to Delta Max Angle which is supplied from block 82. Vds and Vqs are recalculated in block 90 and output at block 92 as noted above. A negative comparison is coupled to block 94 where upon Vqs and Vds experience No Change.

10 The foregoing arrangement is for a motoring mode. Accordingly, if the motor goes to the generating mode, delta and slip frequencies change sign and the comparison becomes a less than calculation in blocks 84 and 110 of Fig. 3

From the foregoing, it can be seen that a new and improved device to regulate current produced by an induction machine has been provided. It is to be
15 understood that the description of the exemplary embodiments is merely illustrative of some of the many specific embodiments that represent applications of the principles of the present invention. Other arrangements would be evident to those skilled in the art without departing from the scope of the invention as defined by the following claims.